the inventive concept, details that are well-known in the art may have been omitted. Nevertheless, those skilled in the art would be able to understand the implementation of the inventive concept and its technical details in view of the present disclosure.

The different embodiments of the inventive concept have been described with reference to the accompanying drawings. However, the different embodiments are merely illustrative and are not intended to limit the scope of the inventive concept. Furthermore, those skilled in the art would appreciate that various modifications can be made to the different embodiments without departing from the scope of the inventive concept.

What is claimed is:

1. A transistor comprising:

a semiconductor substrate comprising a first region and a second region;

an emitter and a base disposed on the first region; and

a collector disposed on the second region,

wherein the emitter is disposed on an upper surface of the semiconductor substrate forming a heterojunction between the emitter and the upper surface of the semiconductor substrate,

wherein the emitter and the base are spaced apart by a stacked layer including at least two different insulating materials, and

wherein a junction between the at least two different insulating materials of the stacked layer has a substantially same height as a height of the heterojunction between the emitter and the upper surface of the semiconductor substrate.

2. The transistor according to claim **1**, wherein the first region is doped with an n-type impurity and the second region is doped with a p-type impurity, the base is doped with the n-type impurity, and a concentration of the n-type impurity in the base is higher than a concentration of the n-type impurity in the first region.

3. The transistor according to claim **2**, wherein the collector is doped with the p-type impurity, and a concentration of the p-type impurity in the collector is higher than a concentration of the p-type impurity in the second region.

4. The transistor according to claim **1**, wherein the base includes phosphorous-doped silicon carbide and the emitter includes boron-doped silicon germanium.

5. The transistor of claim **4**, wherein the collector includes the boron-doped silicon germanium.

6. The transistor according to claim **1**, wherein the first region is doped with a p-type impurity and the second region is doped with an n-type impurity, the base is doped with the p-type impurity, and a concentration of the p-type impurity in the base is higher than a concentration of the p-type impurity in the first region.

7. The transistor according to claim **6**, wherein the collector is doped with the n-type impurity, and a concentration of the n-type impurity in the collector is higher than a concentration of the n-type impurity in the second region.

8. The transistor according to claim **6**, wherein the emitter includes phosphorous-doped silicon carbide.

9. The transistor according to claim **1**, wherein the first region is doped with a p-type impurity and the second region is doped with an n-type impurity; and

the emitter includes boron-doped silicon germanium.

10. The transistor according to claim **9**, wherein the base includes phosphorous-doped silicon carbide.

11. The transistor according to claim **9**, wherein the collector includes the boron-doped silicon germanium.

12. A method of manufacturing a transistor, comprising:

forming a first region and a second region on a semiconductor substrate;

forming an emitter on the first region and a collector on the second region; and

forming a base on the first region,

wherein the emitter is disposed on an upper surface of the semiconductor substrate forming a heterojunction between the emitter and the upper surface of the semiconductor substrate,

wherein the emitter and the base are spaced apart by a stacked layer including at least two different insulating materials, and

wherein a junction between the at least two different insulating materials of the stacked layer has a substantially same height as a height of the heterojunction between the emitter and the upper surface of the semiconductor substrate.

13. The method according to claim **12**, wherein the first region is doped with an n-type impurity and the second region is doped with a p-type impurity, the base is doped with the n-type impurity, and a concentration of the n-type impurity in the base is higher than a concentration of the n-type impurity in the first region.

14. The method according to claim **13**, wherein the collector is doped with the p-type impurity, and a concentration of the p-type impurity in the collector is higher than a concentration of the p-type impurity in the second region.

15. The method according to claim **12**, wherein the base includes phosphorous-doped silicon carbide, and the collector and the emitter include boron-doped silicon germanium.

16. The method according to claim **12**, wherein the first region is doped with a p-type impurity and the second region is doped with an n-type impurity;

and the emitter includes phosphorus-doped silicon carbide.

17. The method of claim **16**, wherein the base is doped with the p-type impurity, and a concentration of the p-type impurity in the base is higher than a concentration of the p-type impurity in the first region.

18. The method according to claim **16**, wherein the collector is doped with the n-type impurity, and a concentration of the n-type impurity in the collector is higher than a concentration of the n-type impurity in the second region.

19. A method of manufacturing a transistor, comprising:

forming a first region and a second region on a semiconductor substrate,

wherein the first region is doped with a p-type impurity and the second region is doped with an n-type impurity;

forming an emitter on the first region and a collector on the second region,

wherein the emitter includes boron-doped silicon germanium; and

forming a base on the first region,

wherein the emitter is disposed on an upper surface of the semiconductor substrate forming a heterojunction between the emitter and the upper surface of the semiconductor substrate,

wherein the emitter and the base are spaced apart by a stacked layer including at least two different insulating materials, and

wherein a junction between the at least two different insulating materials of the stacked layer has a substantially same height as a height of the heterojunction between the emitter and the upper surface of the semiconductor substrate.